Research Progress of Phase Locked Loop and Delay Locked Loop

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Abstract: With the development of SoC technology and IP core technology, the Phase Locked Loop (PLL) which is regarded as a basic ASIC macro cell is widely used as a clock generation circuit in wireless communication and microprocessor circuits. The clock generation circuit is mainly composed of PLL or Delay Locked Loop (DLL). This paper first introduces the basic situation of clock deviation and jitter in modern VLSI system concept. Then, the DLL technology used in clock management is introduced, including the fundamental principle and theoretical analysis of PLL and DLL. The circuit of several common DLLs is analyzed and compared with PLL. Finally, the significance of PLL research is summarized.

1. Introduction

In 1932, phase-locked technology was used in synchronous reception, providing synchronous detection with a local reference signal in phase with the input signal carrier. The popularization of PLLs began in 1943 from black and white TV horizontal sync circuits, which reduced the impact of noise on synchronization and improved the synchronization performance of TV images. After the eighties, phase-locked technology has been widely used in the communications, radar, aerospace, measuring instruments, computers, infrared, laser, atomic energy, television, stereo, motor control and industrial, geological, and other technical departments [1].

As the PLL is widely used in the field of electronic technology, it has gradually become a primary circuit commonly used in electronic equipment [2]. To facilitate adjustment, reduce costs, improve reliability and perform better in a variety of electronic devices, the PLL is eager to be integrated, digital, minimized and generalized. The current integrated PLL has become a significant development of phase-locked technology development.

Many systems require a PLL to generate a clock or oscillation signal. Due to the importance of the timing signal and its sensitivity to noise and interference, the PLLs in these systems or the timing signal generation circuit are critical parts of the overall system. PLL applications include clock data recovery, clock synthesis and synchronization, frequency synthesis and modulation and demodulation [3].

In recent years, DLL has become a solution to the problem of clock adjustment [4]. DLL is based on the fundamental principles of PLL developed, and its function is similar to the PLL, but the performance has been improved. It is easy to integrate and achieve full CMOS circuit. Moreover, it has high reliability, small size, low power consumption; and it also broke through the digital PLL (DPLL) speed limit, can working in hundreds of megahertz frequency. Also, the Delayed Locked Loop has a substantial advantage in reducing clock skew and jitter.

This paper is going to illustrate the basic principle of PLL and DLL. In the following parts, the clock problems will be raised firstly. The next part is about the clock recovery System. Thirdly, some fundamental concepts of PLL and DLL, and the comparisons will be introduced. And the last part of this paper is a brief conclusion of current findings.

2. Clock Problems

Many factors lead to clock problems. The primary source of clock problems is in the process of generating the clock, including the deviations in device manufacturing, and interconnect bias. Ambient temperature, power supply voltage changes, capacitance coupling, and other factors will also lead to the generation of clock problems.

The uncertainty of the clock also has a variety of classification. By error type, it can be divided into system errors and random errors. System errors are the same and predictable between different chips. System errors can be detected by testing a set of chips, and then by adjusting the design to make up. Random errors are caused by the changes in the manufacturing process. And they are difficult to simulate and eliminate. Clock inconsistencies can also be divided into static and time-varying. The temperature gradient on a chip is time-varying, and the power supply noise caused by the flip-flop in the clock network is static, and the effect on each cycle is the same [5,6].

2.1 Clock Jitter

Clock jitter refers to the uncertainty of the period (frequency) of the actual clock or the deviation between the time point of a fixed reference point and the time point of the ideal clock [7]. In the general literature, clock jitter can be divided into three types: Phase jitter, Periodic jitter, and period jitter.

3. Clock Recovery System

Fig. 1 shows the basic structure clock recovery system. We can see from the figure that the external crystal provides a stable 12MHz sine reference frequency signal. Firstly, two inverters generate 12MHz square wave signal, and then the signal is input to the clock multiplier. PLL is used to achieve the clock signal multiplier and frequency and produce a 480MHz frequency of the local clock signal, providing the delay PLL module for external communication U_i clock recovery. The external data is restored by the restored clock, that is, the received data information is recovered from the external communication signal U_i. The frequency signals used by other modules can be divided by the 480MHz clock signal [8].

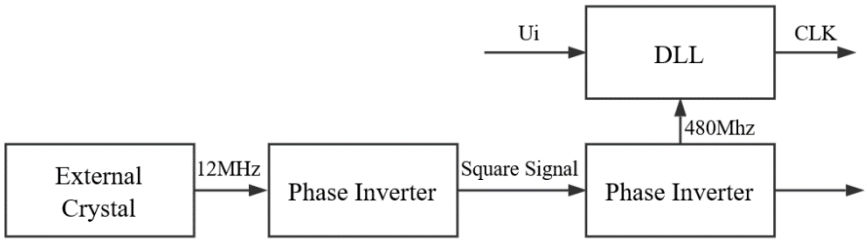

Fig. 1 Flow chart of clock recovery function Basic Content of PLL and DLL

3.1 Basic Principle of PLL

PLL is a closed-loop phase automatic control system, which is based on automatic control theory. It consists of three basic parts: phase detector (PD), the loop filter (LPF) and voltage controlled oscillator (VCO). When the PLL is operated, the PD will compare the phase of the input signal with the phase of the output signal of the VCO (also called the feedback signal). And the detector will output an error signal which varies with the phase difference of the two signals. The error signal is smoothed and amplified by the LPF and then applied to the control terminal of the VCO, to change the frequency and phase of the voltage output of the VCO towards the direction of the phase difference between the two signals. Finally, the frequency difference disappears, and the phase difference is small enough to achieve the purpose of locking (synchronization). This is the fundamental principle of PLLs.

The most basic PLL structure [3] is shown in Fig. 2, including three components: PD, LPF, and VCO. Wherein the PD is a phase comparison means which compares the phase of the input signal V_i and the VCO output signal V_o to generate a phase error voltage V_d corresponding to the phase difference of the two signals. The effect of the LPF is to filter out the high-frequency components and noise in the error voltage V_d to increase the stability of the loop and generate a static phase

error voltage. The VCO is controlled by the controlled voltage V_c so that the output frequency of the VCO is closer to the input signal frequency, making the frequency difference smaller and smaller until the frequency difference is eliminated.

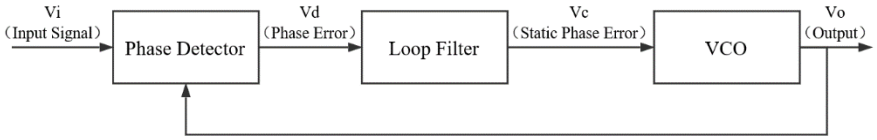

Fig. 2 Structure diagram of basic PLL

3.2 Basic Principle of DLL

Compared with the PLL, the DLL does not change the frequency of the output signal. And it only compares the input signal and the output signal phase. When the difference of output signal phase and input signal phase is less than a specified value, the DLL implementation is considered as locked, so the output signal delays the input signal for an integer cycle [9].

The DLL mainly includes the following four parts: PD, Charge Pump (CP), LPF and Voltage-Controlled Delay Line (VCDL). As shown in Fig. 3, the working principle of the DLL is that the PD detects the phase difference between the input signal (CLKREF) and the output feedback signal (CLKFB). If there is a phase difference between these two signals, the PD will produce a phase difference value with the width of the UP or DN pulse signal, to control the charge pump current ICP to the LPF capacitor charge or discharge, change the size of the control voltage V_{ctrl}, and then adjust the delay time of the voltage control delay line. The voltage-controlled delay line is cascaded by a series of voltage-controlled delay units. The input signal is fed back to the PD via the voltage-controlled delay line and begins the next comparison. This action is repeated until the phase difference between the output feedback signal and the input signal is zero, and then the DLL is locked.

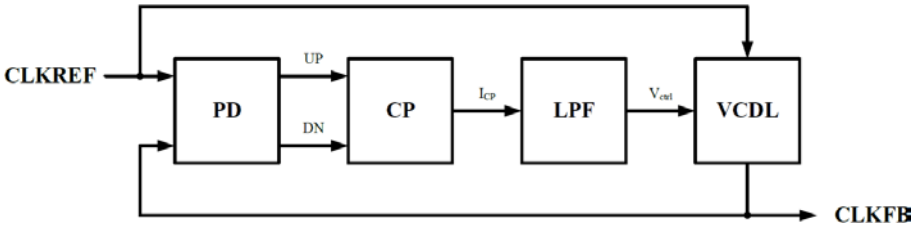

Fig. 3 Framework of DLL principles

3.3 Open-loop DLL and Closed-loop DLL

According to the structure of the loop, DLL can be divided into open-loop DLL and closed-loop DLL. The open loop DLL has no feedback loop, which uses internal delay control to model internal delays (such as receiver input delay, internal buffer delay, etc.), called Synchronous Mirror Delay mode. The closed-loop DLL will store the delay in the register delay and compare the internal clock and external clock phase difference to determine the delay increase or decrease, thus manipulating the register shift. However, this closed-loop structure can accurately locate the clock. And it requires further improvements to shorten the time to enter the lock state.

3.4 The Comparison between PLL and DLL

Compared to the general PLL, DLL has two outstanding advantages:

1) For the VCO, its output frequency is proportional to the input control voltage, and its transfer function contains a pole: $H(s) = K_{VCO}/s$. For the voltage-controlled delay line (VCDL). The output phase is proportional to the input control voltage, and its transfer function is a constant. Therefore, for the first-order LPF, the system transfer function of the PLL based on the voltage-controlled delay line is the first-order equation. This will be easier to consider for gain, bandwidth, and stability than for second-order systems.

2) Smaller phase jitter. Phase jitter is a very important indicator of the PLL, and the noise of the circuit is one of the causes of this jitter. The noise of the input VCO is output by itself, and the noise of the input voltage-controlled delay line disappears through the delay line so that the phase jitter is improved.

DLL and PLL can realize the same basic function of zero delay output and multiplier and

frequency division. Also, they are based on the same principle: compensating and adjusting the difference between the input clock and feedback clock. However, it is hard to overcome the drawback that the VCO itself is unstable. When the oscillator works for a long time, there will be a cumulative phase error. Using it as a benchmark to adjust the input clock will inevitably have errors and will form a deviation accumulated. Unconditionally stable DLL structures do not accumulate phase errors. For the above reasons, when the clock zero delay requirements are higher, the DLL is recommended; and for frequency synthesis, the PLL is a better choice.

3.5 Improved PLL and DLL Based on Self-Biased Techniques

High-performance DLL has the characteristics of wide frequency bandwidth, small phase jitter, and low power consumption. However, it is difficult to achieve these goals. On the one hand, the narrower the bandwidth of the loop, the smaller the jitter; on the other hand, the loop bandwidth and the operating frequency are limited by the loop stability conditions. With the self-biased DLL structure, the bandwidth of the whole system can follow the change of the working frequency, so that the working frequency range of the closed-loop DLL system is only determined by the designed buffer circuit, and has high noise suppression ability. Maneatis's group did a lot of work in the self-biased PLL and DLL techniques [10], they reported that self-biasing avoids the necessity for external biasing, which can require special bandgap bias circuits, by generating all of the internal bias voltages and currents from each other so that the bias levels are completely determined by the operating conditions [11].

4. Conclusion

Although the PLL is relatively simple in structure, it has a wider range of applications in the field of radio electronics because of its outstanding advantages and derives a variety of special circuits with different properties and complex structures. Therefore, the research content is vibrant. As an automatic adjustment system, PLL detection is the phase difference between the two signals, and the item it put control on is the signal phase rather than the voltage amplitude. For the phase difference, the PLL is usually a nonlinear feedback system. Only when the phase difference is small enough, the PLL can be approximately regarded as a linear system to deal with. In the actual work, inevitably there will be some noise and interferences, which make the analysis PLL very complicated and challenging. So there is still a long way to go for the study of PLL in the future.

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